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Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Complete if Known

Application Number	Unknown
Filing Date	Even Date Herewith
First Named Inventor	Geusic, Joseph
Group Art Unit	Unknown 2823
Examiner Name	Unknown MAldonado, J

Sheet 1 of 4

Attorney Docket No: 303.390US4

US PATENT DOCUMENTS

Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	Filing Date If Appropriate
JS	US-3,968,564	07/13/1976	Springthorpe, A. J.	29	580	04/30/1975
JS	US-4,734,384	03/29/1988	Tsuchiya, Osamu	437	52	05/13/2086
JS	US-4,744,623	05/17/1988	Prucnal, P. R., et al.	350	96.20	06/30/1986
JS	US-4,920,070	04/24/1990	Mukai, Ryoichi	437	173	11/27/1987
JS	US-4,970,578	11/13/1990	Tong, Elsa K., et al.	357	81	09/28/1988
JS	US-5,128,831	07/07/1992	Fox III, Angus C., et al.	361	396	10/31/1991
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JS	US-5,362,976	11/08/1994	Suzuki, Katsuhiko	257	81	10/26/1992
JS	US-5,409,563	04/25/1995	Cathey,	156	643	02/26/1993
JS	US-5,416,872	05/16/1995	Sizer II, T., et al.	385	92	07/06/1993
JS	US-5,431,775	07/11/1995	Prince, Eric T.	216	24	07/29/1994
JS	US-5,489,554	02/06/1996	Gates, James L.	437	208	02/04/1994
JS	US-5,532,506	07/02/1996	Tserng, H. Q.	257	276	11/14/1994
JS	US-5,587,119	12/24/1996	White, D. M.	264	104	05/26/1995
JS	US-5,604,835	02/18/1997	Nakamura, T., et al.	385	129	12/22/1994
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JS	US-5,641,545	06/24/1997	Sandhu, G. S.	427	573	06/07/1995
JS	US-5,656,548	08/12/1997	Zavracky, Paul M., et al.	438	23	09/19/1995
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JS	US-5,729,038	03/17/1998	Young, William R., et al.	257	460	12/15/1995
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JS	US-5,858,814	01/12/1999	Goossen, Keith W., et al.	438	107	12/12/1996

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Substitute Disclosure Statement Form (PTO-1449)

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 809. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

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Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)	Complete if Known	
	Application Number	Unknown
	Filing Date	Even Date Herewith
	First Named Inventor	Geusic, Joseph
	Group Art Unit	Unknown
	Examiner Name	Unknown
Sheet 2 of 4	Attorney Docket No: 303.390US4	

	US-5,858,877	01/12/1999	Dennison, C. H., et al.	438	700	01/21/1997
<i>RR</i>	US-5,897,333	04/27/1999	Goossen, Keith W., et al.	438	455	03/14/1997
<i>RR</i>	US-5,900,674	05/04/1999	Wojnarowski, Robert J., et al.	257	774	12/23/1996
<i>RR</i>	US-5,901,050	05/04/1999	Imai, Ryuji	361	820	08/21/1997
<i>RR</i>	US-5,902,118	05/11/1999	Hubner, Holger	438	106	07/03/1995
<i>RR</i>	US-5,903,045	05/11/1999	Bertin, Claude L., et al.	257	621	04/30/1996
<i>RR</i>	US-5,915,167	06/22/1999	Leedy, Glenn J.	438	108	04/04/1997
<i>RR</i>	US-5,952,665	09/14/1999	Bhargava, R. N.	250	483.1	11/28/1997
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<i>RR</i>	JP-04-263462	09/18/1992	Shimizu, Kozo	H01L	25/04	
<i>RR</i>	JP-05-145060	06/11/1993	Maaku, Dorainan J.	H01L	29/44	
<i>RR</i>	JP-56-055067	05/15/1981	Takagi, Y., et al.	H01L	23/52	
<i>RR</i>	WO-91/11833	08/08/1991	Madou, Marc J., et al.	H01 R	9/00	
<i>RR</i>	WO-94/05039	03/03/1994	Capps, David A., et al.	H01L	23/48	

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ⁴
<i>RR</i>		FORBES, L., et al., "Resonant Forward-Biased Guard-Ring Diodes for Suppression of Substrate Noise in Mixed-Mode CMOS Circuits", <u>Electronics Letters</u> , 31, (April 1995), 720-721	

EXAMINER

Julio J. Maldonado

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Substitute Disclosure Statement Form (PTO-1449)

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	Application Number	Unknown
	Filing Date	Even Date Herewith
	First Named Inventor	Geusic, Joseph
	Group Art Unit	Unknown
	Examiner Name	Unknown
Sheet 3 of 4	Attorney Docket No: 303.390US4	

		FOSTER, R. , et al., "High Rate Low-Temperature Selective Tungsten", In: <u>Tungsten and Other Refractory Metals for VLSI Applications III</u> , V.A. Wells, ed., Materials Res. Soc., Pittsburgh, PA,(1988),69-72	
<i>see</i>		GONG, S. , et al., "Techniques for Reducing Switching Noise in High Speed Digital Systems", <u>Proceedings of the 8th Annual IEEE International ASIC Conference and Exhibit</u> , Austin, TX,(1995),21-24	
<i>see</i>		HEAVENS, O. , <u>Optical Properties of Thin Solid Films</u> , Dover Pubs. Inc., New York,(1965),155-206	
<i>see</i>		HORIE, H. , et al., "Novel High Aspect Ratio Aluminum Plug for Logic/DRAM LSI's Using Polysilicon-Aluminum Substitute", <u>Technical Digest: IEEE International Electron Devices Meeting</u> , San Francisco, CA,(1996),946-948	
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<i>see</i>		KLAUS, et al., "Atomic Layer Controlled Growth of SiO2 Films Using Binary Reaction Sequence Chemistry", <u>Applied Physics Lett.</u> 70(9), (3 March 1997),1092-94	
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<i>see</i>		LEHMANN, V. , "The Physics of Macropore Formation in Low Doped n-Type Silicon", <u>Journal of the Electrochemical Society</u> , 140(10), (Oct. 1993),2836-2843	
<i>see</i>		MASU, K. , et al., "Multilevel Metallization Based on Al CVD", <u>1996 IEEE Symposium on VLSI Technology, Digest of Technical Papers</u> , Honolulu, HI,(June 11-13, 1996),44-45	
<i>see</i>		MCCREDIE, B. D. , et al., "Modeling, Measurement, and Simulation of Simultaneous Switching Noise", <u>IEEE Transactions on Components, Packaging, and Manufacturing Technology -- Part B</u> , 19, (Aug. 1996),461-472	
<i>see</i>		MULLER, K. , et al., "Trench Storage Node Technology for Gigabit DRAM Generations", <u>Digest IEEE International Electron Devices Meeting</u> , San Francisco, CA,(Dec. 1996),507-510	
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EXAMINER

Julius H. Adkins

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06/20/05

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Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)	Complete if Known	
	Application Number	Unknown
	Filing Date	Even Date Herewith
	First Named Inventor	Geusic, Joseph
	Group Art Unit	Unknown
	Examiner Name	Unknown
Sheet 4 of 4	Attorney Docket No: 303.390US4	

gc		SENTHINATHAN, R. , et al., "Reference Plane Parasitics Modeling and Their Contribution to the Power and Ground Path "Effective" Inductance as Seen by the Output Drivers", <u>IEEE Transactions on Microwave Theory and Techniques</u> , 42, (Sep. 1994),1765-1773	
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gc		SZE, S M., <u>VLSI Technology</u> , 2nd Edition, Mc Graw-Hill, NY, (1988),90	
gc		VITTAL, A. , et al., "Clock Skew Optimization for Ground Bounce Control", <u>1996 IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers</u> , San Jose, CA,(Nov. 10-14, 1996),395-399	

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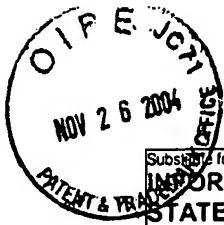
Gregory J. Molodtsov

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2/15/00

Substitute Disclosure Statement Form (PTO-1446)

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Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)	Complete if Known	
	Application Number	10/772,606
	Filing Date	February 5, 2004
	First Named Inventor	Geusic, Joseph
	Group Art Unit	2823
	Examiner Name	Maldonado, Julio
Sheet 1 of 1		Attorney Docket No: 303.390US4

US PATENT DOCUMENTS				
Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Filing Date if Appropriate
<i>JP</i>	US-5,200,631	04/06/1993	Austin, F. D., et al.	08/06/1991
<i>JP</i>	US-5,652,811	07/29/1997	Cook, P., et al.	03/06/1996

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Julio J. Maldonado

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Substitute Disclosure Statement Form (PTO-1449)

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